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| 09/887,021 | 06/25/2001 | Terry R. Lee | M4065.0407/P407 | 6645 |

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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

| EXAMINER | |
|---|---|
| VU, TRISHA U | |

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|---|---|
| 2112 | 3 |

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/887,021 | LEE, TERRY R. | |
| | Examiner | Art Unit | |
| | Trisha U. Vu | 2112 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-35 are presented for examination.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 5-9, 11-12, 14-16, 18-21, 24, 26-27, 29-31, and 33-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Robertson et al. (6,658,530) (hereinafter Robertson).

As to claim 1, Robertson teaches a circuit card (memory module 100) comprising: an integrated circuit having a plurality of inputs and a plurality of outputs (Figs. 1A, 1B); a connector (connector 102) having a plurality of pins (pins 104, 106,...); and a plurality of conductors, each of said plurality of conductors being coupled between one of said plurality of inputs and one of said plurality of pins or one of said plurality of outputs and one of said pins (each of the plurality of signal pins is electrically coupled to a signal trace) (Fig. 1A and col. 3, lines 47-67); said plurality of pins having a first portion for conducting bus signals (signal pins 104) and a second portion for providing a shield (ground pins 106), said pins in said first portion being grouped in a plurality of corresponding pairs, a respective one of said pins in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said

plurality of pins (two signal pins 104 are arranged between a pair of ground pins) (Fig. 2B and col. 4, lines 57-67).

As to claim 2, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 5, Robertson further teaches the integrated circuit is a memory device (col. 4, lines 5-21).

As to claim 6, Robertson teaches a circuit card comprising: a connector (connector 102) having a plurality of pins (pins 104, 106,...); a plurality of conductors, each of said plurality of conductors being coupled to one of said plurality of pins (each of the plurality of signal pins is electrically coupled to a signal trace); and an integrated circuit having a plurality of inputs and a plurality of outputs (Figs. 1A, 1B), said conductors being coupled between one of said plurality of inputs and one of said plurality of pins or one of said plurality of outputs and one of said plurality of pins (Fig. 1A and col. 3, lines 47-67); said plurality of pins having a first portion for conducting bus signals (signal pins 104) and a second portion for providing a shield (ground pins 106), said pins in said first portion being grouped in a plurality of corresponding pairs, a respective one of said pins in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of pins (two signal pins 104 are arranged between a pair of ground pins) (Fig. 2B and col. 4, lines 57-67).

As to claim 7, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 8, Robertson teaches a circuit card comprising: a first plurality of conductive traces to conduct signals (each of the plurality of signal pins is electrically coupled to a signal trace), said first plurality of conductive traces being grouped in a plurality of corresponding pairs (pair of signals); and a second plurality of conductive traces to provide a shield (ground), a respective one of said second plurality of conductive traces being located on each side of each of said plurality of corresponding pairs of said first plurality of conductive traces; wherein said first plurality of conductive traces are part of a bus system (two signal pins 104 are arranged between a pair of ground pins) (Figs. 1A, 1B, 2B and col. 4, lines 57-67).

As to claim 9, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 11, Robertson teaches a memory expansion card (memory module 100) comprising: a memory device having a plurality of inputs and outputs (Figs. 1A, 1B); and a connector having a plurality of pins (connector 102 with pins 104, 106,...), each of said plurality of inputs and output of said memory device being coupled to at least one of said plurality of pins to receive signals from or send signals to said pins of said connector, a first portion of said plurality of pins for conducting signals (signal pins 104) and a second portion of said plurality of pins for providing a shield (ground pins 106), said pins in said first portion being grouped in a plurality of corresponding pairs, a respective one of said pins in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of pins; wherein

said first portion of said plurality of pins is part of a bus system (two signal pins 104 are arranged between a pair of ground pins) (Figs. 1A, 1B, 2B and col. 4, lines 57-67).

As to claim 12, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 14, Robertson further teaches the connector is adapted for connection to a motherboard (col. 3, lines 47-66 and col. 4, lines 40-59).

As to claim 15, teaches a memory expansion card (memory module 100) comprising: a memory device having a plurality of inputs and a plurality of outputs (Figs. 1A, 1B); a first plurality of conductive traces to conduct signals to said plurality of inputs or from said plurality of outputs (each of the plurality of signal pins is electrically coupled to a signal trace), said first plurality of conductive traces being grouped in a plurality of corresponding pairs (signals); and a second plurality of conductive traces to provide a shield (ground), a respective one of said second plurality of conductive traces being located on each side of each of said plurality of corresponding pairs of said first plurality of conductive traces; wherein said first plurality of conductive traces are part of a bus system (two signal pins 104 are arranged between a pair of ground pins) (Figs. 1A, 1B, 2B and col. 4, lines 57-67).

As to claim 16, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 18, teaches a connector comprising (connector 102): a plurality of pins (pins 104, 106,...), said plurality of pins having a first portion for conducting signals (signal pins 104) and a second portion for providing a shield (ground pins 106), said pins

in said first portion being grouped in a plurality of corresponding pairs, a respective one of said pins in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of pins; wherein said first portion of pins is part of a bus system (two signal pins 104 are arranged between a pair of ground pins) (Figs. 1A, 1B, 2B and col. 4, lines 57-67).

As to claim 19, teaches a processing system comprising: a processing unit (CPU 1001); and a circuit card (memory module 100) coupled to said processing unit (Figs. 4, 5), said circuit card comprising: an integrated circuit having a plurality of inputs and a plurality of outputs (Figs. 1A, 1B); a connector having a plurality of pins (connector 102 with pins 104, 106,...); and a plurality of conductors, each of said plurality of conductors being coupled between one of said plurality of inputs and one of said plurality of pins or one of said plurality of outputs and one of said plurality of pins (each of the plurality of signal pins is electrically coupled to a signal trace); said plurality of pins having a first portion for conducting signals (signal pins 104) and a second portion for providing a shield (ground pins 106), said pins in said first portion being grouped in a plurality of corresponding pairs, a respective one of said pins in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of pins (two signal pins 104 are arranged between a pair of ground pins) (Figs. 1A, 1B, 2B and col. 4, lines 57-67); wherein said processing system comprises a bus system for passing signals through said processing system and said first portion of said plurality of pins are coupled to said bus system (Figs. 4, 5, and col. 5 lines 40-67).

As to claim 20, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 21, Robertson further teaches each of said plurality of inputs and plurality of outputs of said integrated circuit are coupled to a plurality of pins of said connector (signals from/to connector 102) (Figs. 1A, 1B).

As to claim 24, Robertson further teaches said integrated circuit is a memory device (col. 4, lines 5-21).

As to claim 26, teaches a processing system comprising: a processing unit (CPU 1001); and a memory expansion card coupled to said processing unit (Figs. 4, 5), said memory expansion card (memory module 100) comprising: a memory device having a plurality of inputs and a plurality of outputs (Figs. 1A, 1B); and a connector having a plurality of pins (connector 102 with pins 104, 106,...), each of said plurality of inputs and said plurality of outputs of said memory device being coupled to at least one of said plurality of pins to receive signals from or send signals to said pins of said connector (Figs. 1A, 1B), a first portion of said plurality of pins for conducting signals (signal pins 104) and a second portion of said plurality of pins for providing a shield (ground pins 106), said pins in said first portion being grouped in a plurality of corresponding pairs, a respective one of said pins in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of pins (two signal pins 104 are arranged between a pair of ground pins) (Figs. 1A, 1B, 2B and col. 4, lines 57-67); wherein said processing system comprises a bus system for passing signals

through said processing system and wherein said first portion of said plurality of pins are coupled to said bus system (Figs. 4, 5, and col. 5 lines 40-67).

As to claim 27, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 29, Robertson further teaches a motherboard, wherein said connector is adapted for connection to said motherboard (col. 3, lines 47-66 and col. 4, lines 40-59).

As to claim 30, teaches a processing system comprising: a processing unit (CPU 1001); and a memory expansion card (memory module 100) coupled to said processing unit (Figs. 4, 5), said memory expansion card comprising: a memory device having a plurality of inputs and a plurality of outputs (Figs. 1A, 1B); a first plurality of conductive traces to conduct signals to said plurality inputs or from said plurality of outputs (each of the plurality of signal pins is electrically coupled to a signal trace), said first plurality of conductive traces being grouped in a plurality of corresponding pairs (signals); and a second plurality of conductive traces to provide a shield (ground), a respective one of said second plurality of conductive traces being located on each side of each of said plurality of corresponding pairs of said first plurality of conductive traces; wherein said first plurality of conductive traces are part of a bus system of said processing system (two signal pins 104 are arranged between a pair of ground pins) (Figs. 1A, 1B, 2B and col. 4, lines 57-67).

As to claim 31, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 33, teaches a method for constructing a circuit card for a bus system comprising the steps of: providing a first plurality of pins on a connector of said circuit card (connector 102 with pins 104, 106,...), said first plurality of pins for conducting bus signals (signal pins 104); grouping said first plurality of pins into a plurality of corresponding pairs; providing a second plurality of pins on said connector of said circuit card, said second plurality of pins for providing a signal shield (ground pins 106); and locating a pin of said second plurality of pins adjacent to each side of said corresponding pairs of pins of said first plurality of pins (two signal pins 104 are arranged between a pair of ground pins) (Figs. 1A, 1B, 2B and col. 4, lines 57-67).

As to claim 34, Robertson further teaches coupling each of said second plurality of pins to a ground potential (ground) (col. 3, lines 62-67).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson et al. (6,658,530) (hereinafter Robertson) in view of Chin et al. (6,216,205) (hereinafter Chin).

As to claim 3, the argument above for claim 1 applies. However, Robertson does not explicitly disclose a driver to drive the signals between said inputs and said outputs of said integrated circuit memory device. Chin teaches driver (I/O driver 16) to drive signals between inputs and outputs of an integrated circuit memory device (col. 8, lines 28-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a driver as taught by Chin in the integrated circuit memory device of Robertson to for transferring data to and from the memory device (col. 8, lines 32-39).

As to claim 22, the argument above for claim 19 applies. However, Robertson does not explicitly disclose a driver to drive the signals between said inputs and said outputs of said integrated circuit memory device. Chin teaches driver (I/O driver 16) to drive signals between inputs and outputs of an integrated circuit memory device (col. 8, lines 28-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a driver as taught by Chin in the integrated circuit memory device of Robertson to for transferring data to and from the memory device (col. 8, lines 32-39).

4. Claims 4, 10, 13, 17, 23, 28, 32, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson et al. (6,658,530) (hereinafter Robertson) in view of Ortega et al. (6,527,587) (herein after Ortega).

As to claim 4, the argument above for claim 1 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential

signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 10, the argument above for claim 8 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 13, the argument above for claim 11 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 17, the argument above for claim 15 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 23, the argument above for claim 19 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 28, the argument above for claim 26 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 32, the argument above for claim 30 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 35, the argument above for claim 33 applies. Robertson further teaches grouping said first plurality of pins into a plurality of corresponding pairs (Figs. 1A, 1B, 2B and col. 4, lines 57-67). However, Robertson does not explicitly disclose the pins in each corresponding part are adapted to conduct differential signals. Ortega

teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

5. Claims 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson et al. (6,658,530) (hereinafter Robertson) in view of Elabd (6,526,462).

As to claim 25, the argument above for claim 19 applies. However, Robertson does not explicitly disclose the processing unit and the integrated circuit are on a same chip. Elabd teaches implementing the processor, memory, control unit, etc... on the same chip (col. 1, lines 22-54). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the processor and the integrated circuit on the same chip as taught by Elabd in the system of Robertson to provide a product that is smaller and faster (col. 1, lines 26-31).

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses minimizing electrical interference and cross-talk among signal contacts:

| | | |
|---|---|---|
| US Patent | 6,540,559 | Kemmick et al. |
| US Patent | 5,176,538 | Hansell III et al. |

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

Trisha U. Vu
Examiner
Art Unit 2112

uv

Sumati Lefkowitz

SUMATI LEFKOWITZ
PRIMARY EXAMINER